

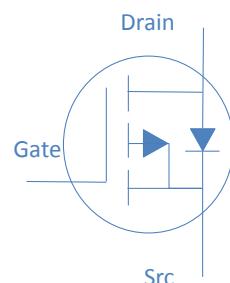
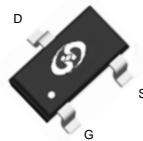
20V P-Ch Power MOSFET
Feature

- ◊ High Speed Power Switching, Logic Level
- ◊ Enhanced Avalanche Ruggedness
- ◊ Lead Free, Halogen Free

V_{DS}	-20	V
$R_{DS(on),typ}$	$V_{GS}=4.5V$	37 mΩ
$R_{DS(on),typ}$	$V_{GS}=2.5V$	55 mΩ
$R_{DS(on),typ}$	$V_{GS}=1.8V$	65 mΩ
I_D (Silicon Limited)	-4	A

Application

- ◊ Load Switches
- ◊ Hard Switching and High Speed Circuit
- ◊ BLDC Motor

SOT-23


Part Number	Package	Marking
HTJ440P02	SOT-23	20

Absolute Maximum Ratings at $T_j=25^\circ C$ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	$T_A=25^\circ C$	-4	A
		$T_A=70^\circ C$	-3	
Drain to Source Voltage	V_{DS}	-	-20	V
Gate to Source Voltage	V_{GS}	-	± 12	V
Pulsed Drain Current	I_{DM}	-	-16	A
Power Dissipation	P_D	$T_A=25^\circ C$	1.25	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to 150	°C

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	100	°C/W
Thermal Resistance Junction-Lead	$R_{\theta JL}$	55	°C/W

Electrical Characteristics at $T_j=25^\circ\text{C}$ (unless otherwise specified)
Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}}=0\text{V}, I_D=-250\mu\text{A}$	-20	-	-	V
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{GS}}=V_{\text{DS}}, I_D=-250\mu\text{A}$	-0.3	-0.75	-1.0	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=-16\text{V}, T_j=25^\circ\text{C}$	-	-	-1	μA
		$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=-16\text{V}, T_j=125^\circ\text{C}$	-	-	-10	
Gate to Source Leakage Current	I_{GSS}	$V_{\text{GS}}=\pm 12\text{V}, V_{\text{DS}}=0\text{V}$	-	-	± 100	nA
Drain to Source on Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}}=-4.5\text{V}, I_D=-4\text{A}$	-	37	44	$\text{m}\Omega$
		$V_{\text{GS}}=-2.5\text{V}, I_D=-3\text{A}$		55	70	
		$V_{\text{GS}}=-1.8\text{V}, I_D=-1\text{A}$	-	65	90	
Transconductance	g_{fs}	$V_{\text{DS}}=-5\text{V}, I_D=-4\text{A}$	-	14	-	S

Dynamic Characteristics

Input Capacitance	C_{iss}	$V_{\text{GS}}=0\text{V}, V_{\text{DS}}=-10\text{V}, f=1\text{MHz}$	-	679	-	pF
Output Capacitance	C_{oss}		-	124	-	
Reverse Transfer Capacitance	C_{rss}		-	106	-	
Total Gate Charge	Q_g	$V_{\text{DD}}=-10\text{V}, I_D=-4\text{A}, V_{\text{GS}}=-4.5\text{V}$	-	12.8	-	nC
Gate to Source Charge	Q_{gs}		-	2.2	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	4.1	-	
Turn on Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}}=-10\text{V}, I_D=-1\text{A}, V_{\text{GS}}=-4.5\text{V}, R_G=6\Omega,$	-	10	-	ns
Rise time	t_r		-	18	-	
Turn off Delay Time	$t_{\text{d}(\text{off})}$		-	32	-	
Fall Time	t_f		-	22	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	$V_{\text{GS}}=0\text{V}, I_F=-3\text{A}$	-	-	-1.2	V
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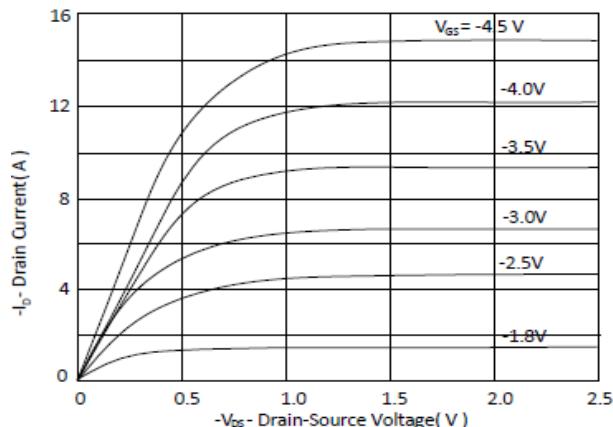
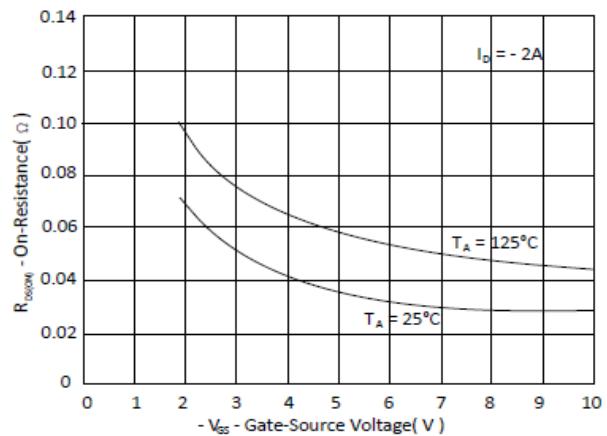
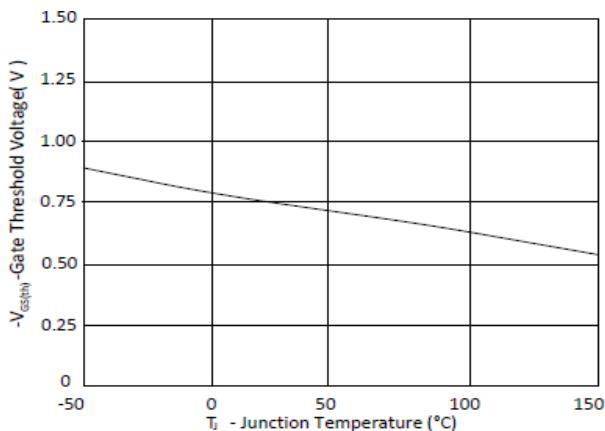
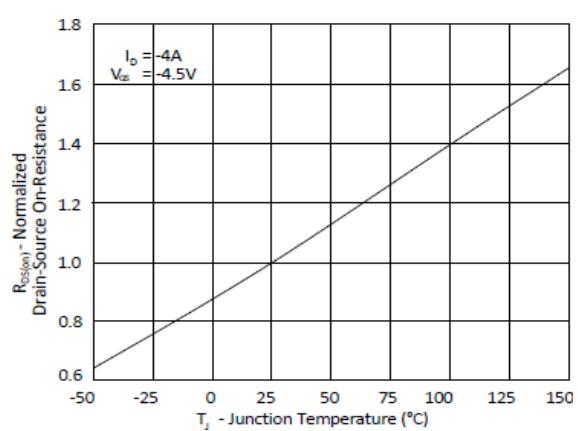
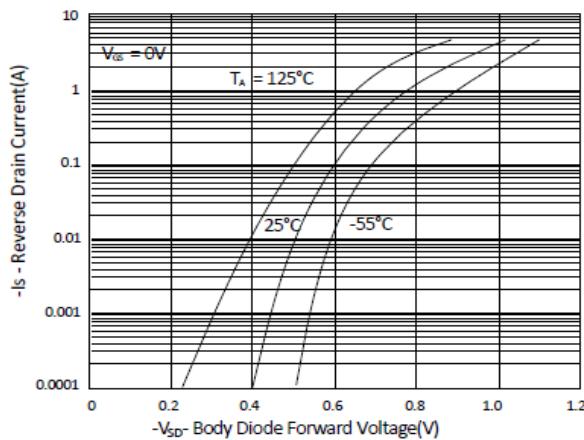
Fig 1. Typical Output Characteristics

Figure 2. On-Resistance vs. Gate-Source Voltage

Figure 3. Gate Threshold Voltage v.s. Junction Temperature

Figure 4. Normalized On-Resistance vs. Junction Temperature

Figure 5. Typical Source-Drain Diode Forward Voltage


Figure 6. Typical Gate-Charge vs. Gate-to-Source Voltage

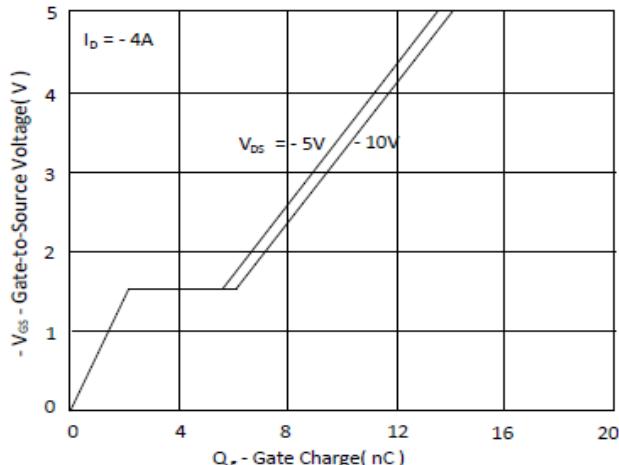


Figure 7. Typical Capacitance vs. Drain-to-Source Voltage

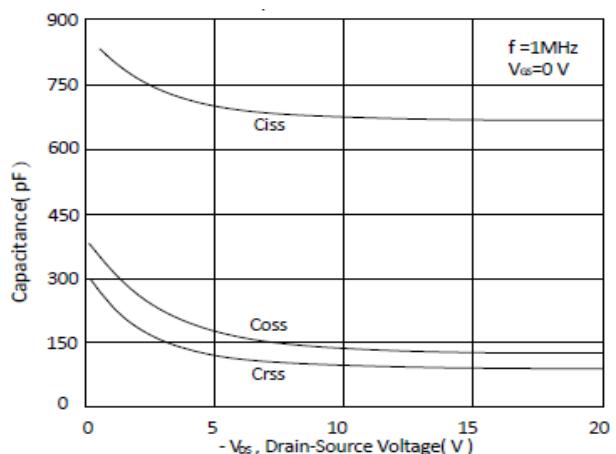


Figure 8. Maximum Safe Operating Area

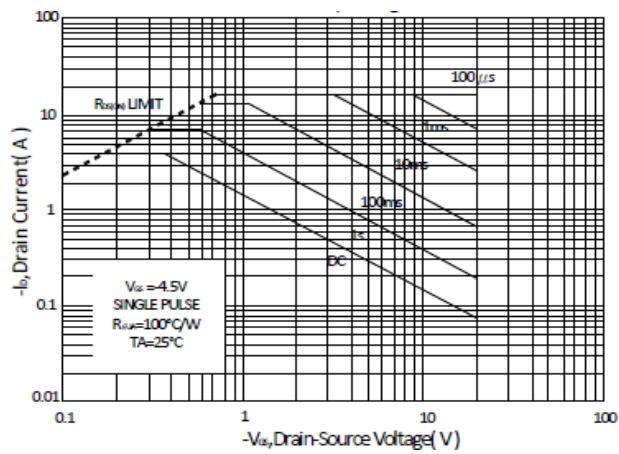


Figure 9. Maximum Drain Current vs. Case Temperature

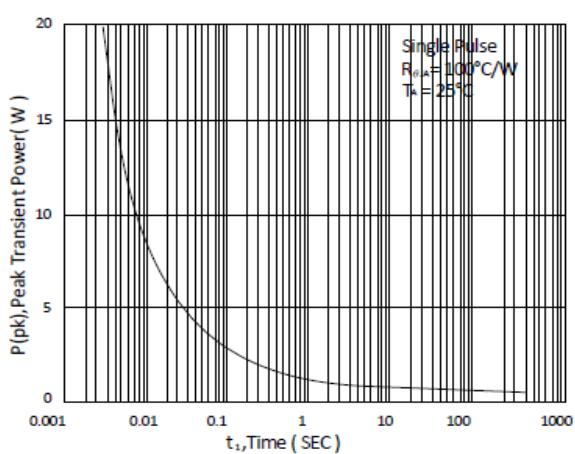
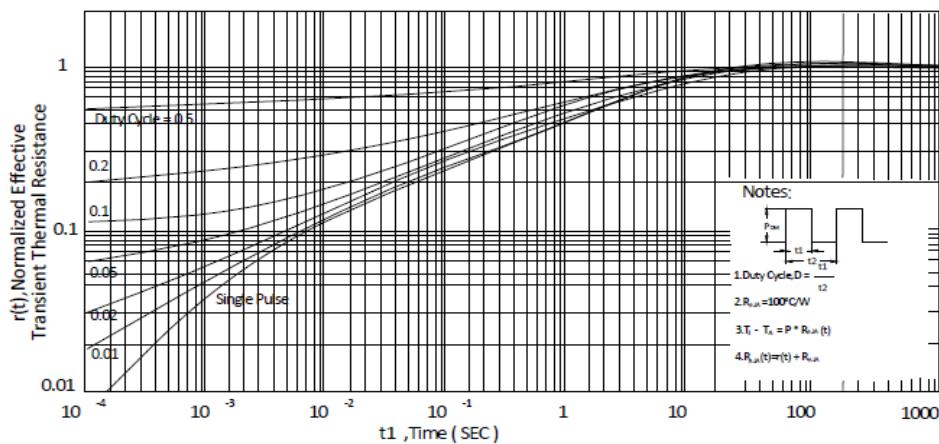
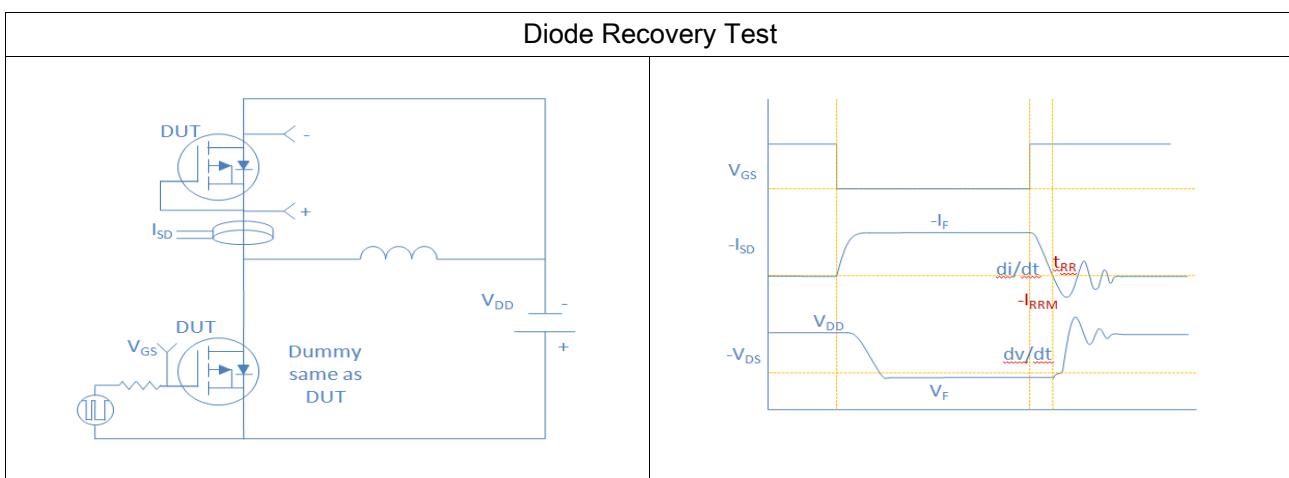
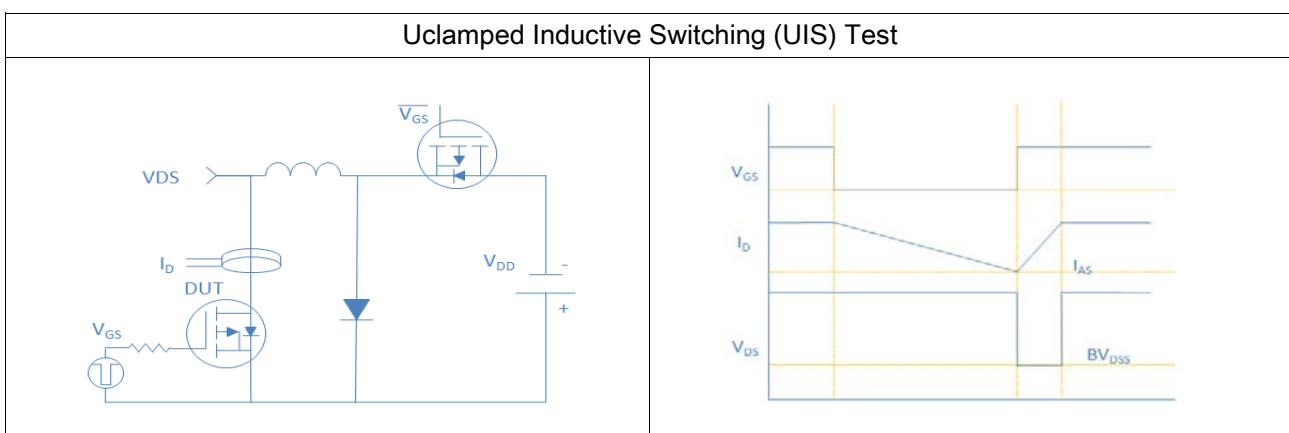
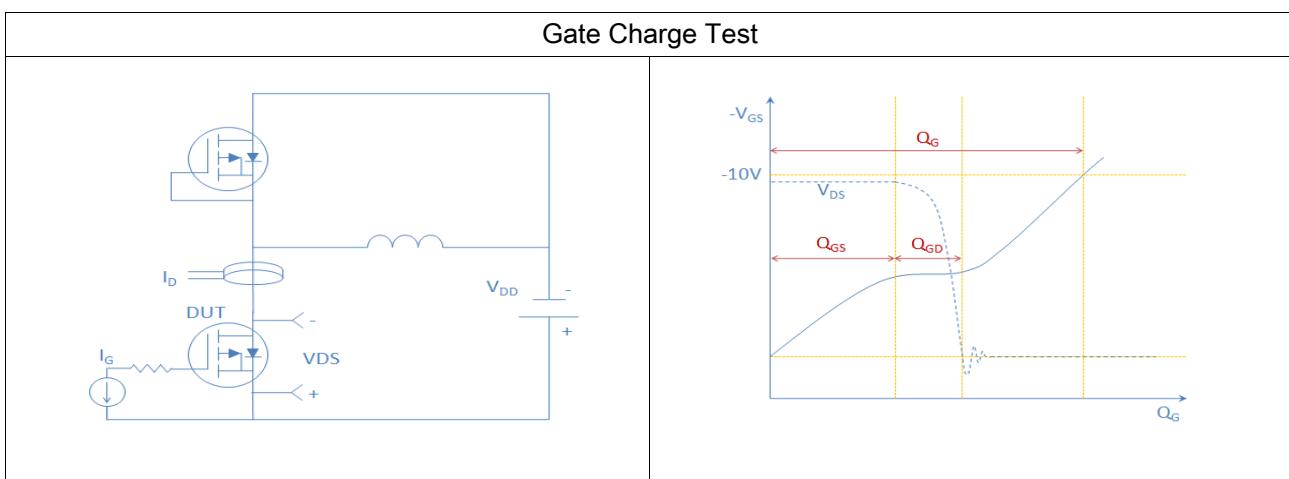
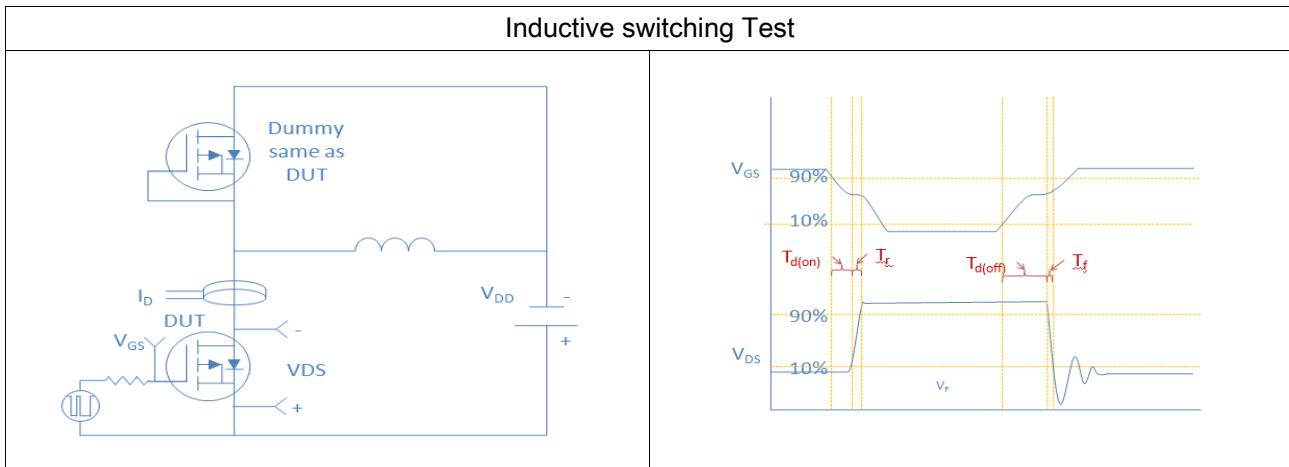
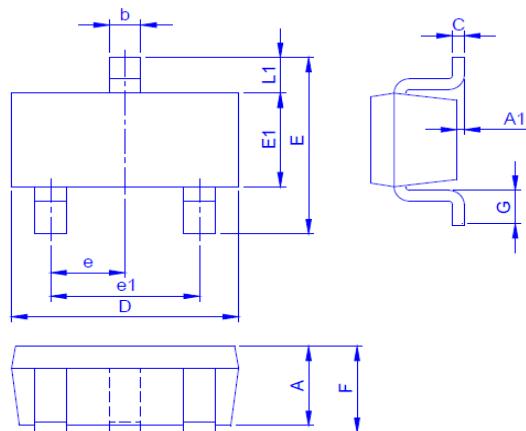


Figure 10. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient





Package Outline
SOT-23, 3leads

Dimension in mm

Dimension	A	A1	A2	b	C	D	E	E1	e	e1	F	G	L1
Min.	0.7	0		0.35	0.1	2.8	2.6	1.5	0.9		0.8	0.3	0.55
Typ.						2.9	2.8	1.6	0.95	1.9			
Max.	1.12	0.1		0.5	0.2	3	3	1.7	1		1.2	0.6	0.65